

AMWAS'07 - Program

Monday 8 October: School

Location: THALES University Jouy en Josas , 67 rue Charles de Gaulle

8.45 - 9.00	G. Edelin (TALES R&T) C. Gamrat (CEA-LIST)	Introduction & Welcome: AMWAS'07 opening
9.00 - 11.00	K. Bertels (TU-Delft, NL)	Polymorphic processor and data-parallel mapping
11.00 - 11.15	Break	
11.15 - 12.30	M. Lankamp (UV-Amsterdam, NL)	SVP- a concurrent method of program composition (part I)
12.30 - 13.30	Lunch	
13.30 - 14.30	M. Lankamp (UV-Amsterdam, NL)	SVP- a concurrent method of program composition (part II)
14.30 - 15.30	A. Shafarenko (Hertfordshire University, UK)	Stream processing and S-Net (part I)
15.30 - 16.00	Break	
16.00 - 17.00	A. Shafarenko (Hertfordshire Univeristy, UK)	Stream processing and S-Net (part II)
17.00 - 17.30	Summary Session	

Tuesday 9 October: School

Location: THALES University Jouy en Josas , 67 rue Charles de Gaulle

9.00 - 10.00	C. Gamrat (CEA-LIST, F)	Heterogeneous Computing Architecture: a key for Adaptive and Self-Adaptive Computers
10.00 - 10.30	Break	
10.30 - 11.30	S. Guyetant (CEA-LIST, F)	Hardware Technologies for Adaptive and Self-Adaptive Computing
11.30-12.30	D. Picard (Univ. de Bret. Occ., F)	Coarse grain reconfigurable technology
12.30 - 13.30	Lunch	
13.30 - 14.30	E. Lenormand (THALES R&T, F)	SPEAR parallel application mapping tool
14.30 - 15.30	M. Hübner (University Karlsruhe, D)	Design Methods and Architectures for Run-Time Adaptive Electronic Systems (Part I)
15.30 - 16.00	Break	
16.00 - 17.00	M. Hübner (University Karlsruhe, D)	Design Methods and Architectures for Run-Time Adaptive Electronic Systems (Part II)
17.00 - 17.30	Summary Session	

Wednesday 10 October: Workshop,

Location: CAP15, 1-13 quai de Grenelle Paris 15, Métro Line 6 - Bir-Hakeim

8.30	Registration	
9.00	G. Edelin (Thales RT), C. Gamrat (CEA-LIST) Welcome Address	
9.15	P. Van Hove (European Commission)	Address to the FET-ACA community
9.30	Dr. S. Singh (Microsoft Research, UK)	Programming Models for Reconfigurable Systems
10.10	Break	
10.30	<i>SESSION 1 - MODEL ENVIRONMENT FOR SELF-ADAPTIVE SYSTEMS</i>	
10.30	A. Grasset (THALES, F)	A framework for memory-based mapping of accelerated function
11.00	M. Lankamp (University Amsterdam, NL)	A Sane Virtual processor implementation and simulation
11.30	D. Picard (Univ. de Bret. Occ., F)	Process Networks on a reconfigurable SoC
12.00	A. Shafarenko (University Hertfordshire, UK)	Extending the S-Net Type System
12.30	Lunch	
14.00	<i>SESSION 2 - PRACTICAL HW AND APPLICATION ISSUES</i>	
14.00	U. Pross (TU Chemnitz, D)	Prototype of a dynamically reconfigurable network
14.30	A. Taddeo (University Lugano, CH)	Security in Self adaptive Systems

15.00	J Kadlec (University Prague, CZ)	UTIA HW platform
15.30	M. Kühnle (University Karlsruhe, D)	A System on chip decoder
16.00	Break	
16.20	EUROPEAN PROJECTS SESSIONS	
16.20	P.S. Paolucci (ATMEL Roma, I)	SHAPES European Project overview
16.55	K. Bertels (TU-Delft, NL)	SARC European Project overview
17.30	G. Pulini (M2000, F)	The M2000 FPGA - A New Direction in FPGA Architectures
17.50	Round Table Session	
	<i>Future ICT Systems: From Tera ops to Tera processor on chip. What are the main challenges ?</i> Animated by J.L. Dormoy (CEA DRT, F)	
19.00 – 21.00	Cocktail Event in CAP15 Pyramid	

Thursday 11 October:

Location: CAP15, 1-13 quai de Grenelle Paris 15, Métro Line 6 - Bir-Hakeim

9.00	SESSION 3 – SELF-ADAPTIVE SYSTEMS : USER INTERFACE	
9.00	L. Lagadec (Univ. de Bret. Occ., F)	Portable synthesis in Morpheus
9.30	F. Muhammad (CNRS, F)	Dynamic and Self adaptive Resource Management: ÆTHER Operating Environment
10.00	M. Van Tol (University Amsterdam, NL)	An implementation of the SANE Virtual Processor using POSIX threads

10.30	Break	
10.45	SESSION 4 - ARCHITECTURE ISSUES FOR SELF-ADAPTATION	
10.45	J. Cabestany (Univ Politecnica Catalunya, E)	A Programmable Hardware Architecture with self-adaptive features
11.15	K. Paulsson (Karlsruhe University, D)	On-line routing of reconfigurable functions for future self-adaptive systems
11.45	E. Schüler (PACT XPP, D)	XPP-III Basics and SoC integration
15.30	J.-M. Philippe (CEA-LIST, F)	The SANE Concept and its Implementation on Reconfigurable Hardware
12.45	Lunch	
14.00	SESSION 5 - SYSTEMS CONCEPTS	
14.00	S. Whitty (TU Braunschweig, D)	High Speed DDR-SDRAM Memory Controller for the MORPHEUS Platform
14.30	C. Teodorov (Univ. de Bret. Occ., F)	Quick integration of high level tools in MORPHEUS: The case of SpecEdit
15.00	K. Bousias (University Amsterdam, NL)	Hardware Design and Implementation of Microthreaded Processors
15.30	L. Lagadec (Univ. de Bret. Occ., F)	Mapping to a reconfigurable IP
16.00	Break	
16.15	Wrap-up and Workshop closing address	